EE 264 Microprocessor Systems and Interfacing – Final **Name:** _____

You have two hours to complete this test.

1. Answer the following short questions about the 68HC11.

16

4 a. Which registers are 16 bits wide?

D, X, Y, (SP), (PC) 1 pt ea

4 b. How wide are the address and data buses?

16 8

4 c. How much memory can the 68HC11 address?

64K x 8

4 d. What is special about memory addresses $1000 - $103F?

Special-Purpose Registers

16 2. Draw a flowchart for the following subroutine:

Compare the contents of memory location $3000 to the contents of memory location $3080. If [$3000] < [$3080] then increment memory location $3100, else set [$3080] equal to [$3000]. Save and restore all registers that are used in the subroutine.

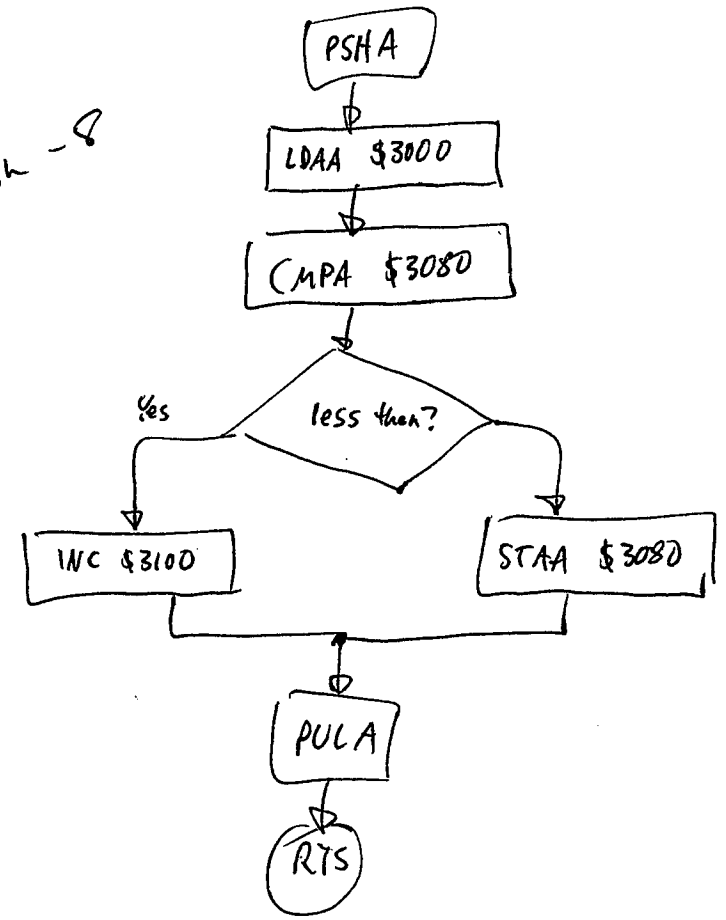
A

No save/restore: -3

gibberish: -12

good start then gibberish -8

1 pt/comment



No RTS: -1

3. Design an interrupt service routine to perform the following operation.

a. What steps are needed to make sure that an interrupt is being used correctly?

6

- Set up interrupt vector
- Put ISR @ vector — init stack
- Enable interrupts
- Enable specific interrupt

] ok if combined

In ISR
- Clear interrupting condition
- use RTI to get back

1 pt each

b. Write a complete program to do the following: When a timer overflow event occurs, clear the timer overflow flag and increment memory location $C200. The main program should start at location $C000. (Hints: What instruction should always be at the end of an interrupt service routine? What goes in the main part and in the service routine?)

10

TOF: Interrupt Vector: $FFDE TOF Flag: $1025 Bit 7 (Most significant bit) TOF Interrupt Enable: $1024 Bit 7 Clear Flag: Write a 1 to TOF Flag

```
        ORG  $FFDE
        FDB  TOF_ISR
        ORG  $C000
        LDAA #$80
        STAA $1024
        CLI
LOOP    BRA  LOOP

TOF_ISR LDAA #$80
        STAA $1025
        INC  $C200
        RTI
```

1 pt per comment

4. Consider the following assembly-language program.
Starting values: [A] = $30, [B] = $10, [X] = $C300, [$C300] = $02, [$C301] = $C3, [$C302] = $00

PSHX	
LDX $C301 ; Note the absence of '#'	X ← C300
LDAA 1,X	A ← C3
ABA	A ← D3
STAA $C300	D3 → [$C300]
PULX	X ← C300

What are the final values of the following registers and memory locations?

[A] = D3 [B] = 10 [X] = C300

[$C300] = D3 [$C301] = C3 [$C302] = 00

18 total
3 each

5. An engineer wants to use the 68HC11 serial port to communicate. The engineer wants to support three baud rates, 76800, 38400, and 9600.

a. What crystal frequency should the engineer select? (Which crystal frequency will let the engineer use the highest baud rate listed above?)

4.9152 MHz

b. Is there a single setting of the SCP1 and SCP0 bits that will cover all baud rates? What should the setting be?

Yes, 00

c. Consider the serial port running at 38400 bits per second. The 68HC11 is using one start bit, one stop bit, and 8 data bits. What is the time to transmit one character?

$1 \text{ bit} = \frac{1}{38400}$ s $\quad 10 \text{ bits} = \frac{10}{38400}$ s $= 260\,\mu s$

off by 10^{-2}

6. Show how to connect the following RAM chip to the 68HC11. The chip is 8 kBytes in size and will occupy memory locations $2000 to $3FFF in the memory map of the 68HC11.

   a. How many address bits does the chip have?

~~15~~ 5

15

8 k Bytes = 13 bits of addr

   b. What is the bit pattern of the most significant address bits that indicates an access to the RAM chip? (That is, what pattern of address bits is always asserted when RAM is being accessed?)

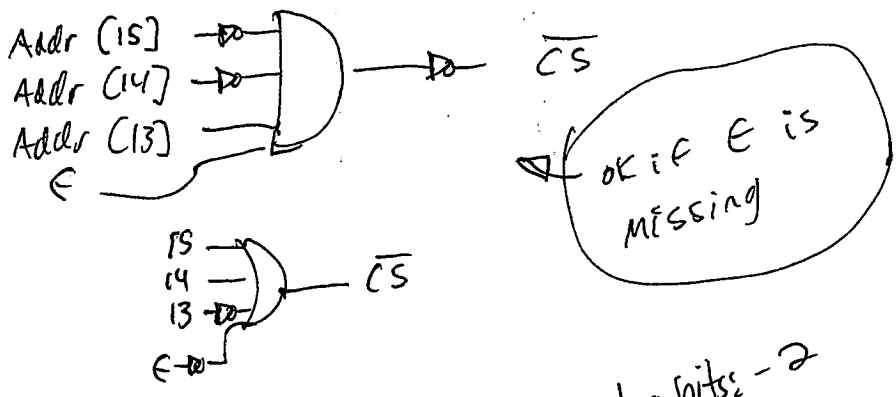
5

001X XXXX XXXX XXXX

Left out a bit -2

   c. Draw a diagram of a logic gate that can use the bit pattern you found in part 'c' to drive the active-low chip select for the RAM part.

5



extra bits: -2

used decoder incorrectly
-4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

EE 264 Microprocessor Systems and Interfacing – Final **Name:** _____

You have two hours to complete this test.

1. Answer the following short questions about the 68HC11. 4pts each

16 a. What does the "HC" refer to?

High Speed CMOS - Logic family

b. How many bits wide are the A, B, D, X, and Y registers?

A, B: 8

D, X, Y: 16

c. Which registers are considered "index registers"?

X and Y extras: −2

d. What register is incremented and decremented when using the PUSH and PULL instructions?

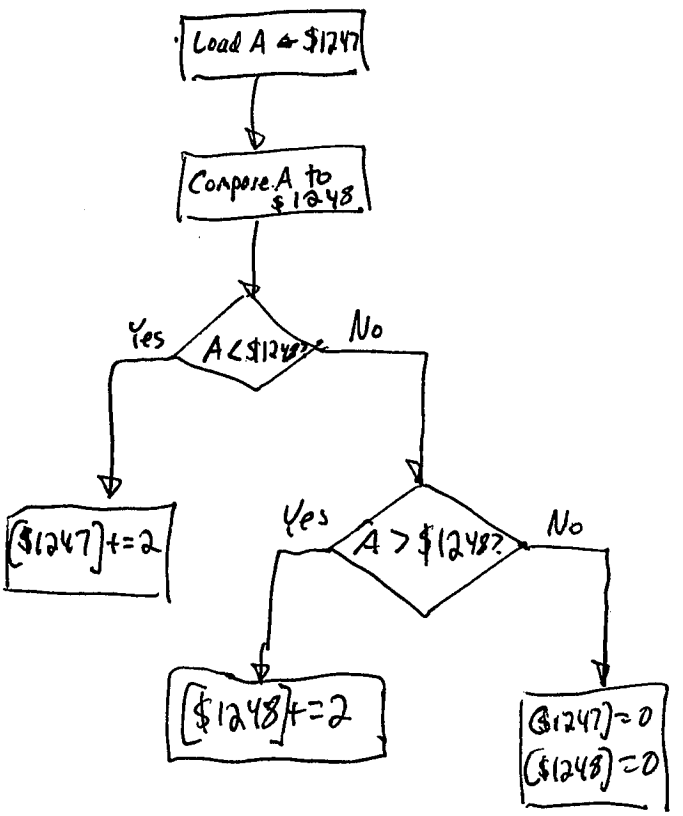
SP

16 2. Draw a flowchart for the following subroutine.

Compare the contents of memory location $1247 to the contents of memory location $1248.

- If [$1247] is less than [$1248], add 2 to [$1247]. (Remember that [$1247] means "the *contents* of memory location $1247")
- If [$1248] is less than [$1247], add 2 to [$1248].
- If the two memory locations are equal, set them both to 0.

3pts per correction



3. Consider the following assembly-language program. 18 pts

Starting values: [A] = $87, [B] = $14, [X] = $C300, [$C300] = $C3, [$C301] = $01, [$C302] = $A0

		A	B	X	C300	C301	C302
	PSHX		14		C3	01	
	LDX $C300			C301			
	LDAA 1,X	A0					
	ABA	B4					
	STAA $C300				B4		
	BSET 0,X $F0					F1	
	CMPB #$14						
	BEQ NXT						
	INCB						
NXT	INCA	B5					
	PULX			C300			

What are the final values of the following registers and memory locations?

[A] = $B5 [B] = $14 [X] = $C300 3 pts each 1 nibble off: -1

[$C300] = $B4 [$C301] = $F1 [$C302] = $A0

4. An engineer wants to use the 68HC11 serial port to communicate. The engineer wants to support three baud rates, 32,768 bps, 8192 bps, and 4096 bps. ~4 pts each

16

a. What crystal frequency should the engineer select? (Which crystal frequency will let the engineer use the highest baud rate listed above?)

2^{23} Hz $(2^{33} - 0)$

b. Is there a single setting of the SCP1 and SCP0 bits that will cover all baud rates? What should the setting be?

00
OR
10

c. Consider the serial port running at 8192 bits per second. What is the time to transmit one bit?

$\frac{1}{8192}$ s = 122 μs off by 10^{i} -2

d. For each character, the 68HC11 typically sends one start bit, 8 data bits, no parity bits, and one stop bit. At 8192 bits per second, how long does it take to transmit one character?

$\frac{10}{8192}$ s = 1.22 ms extra bit -1

5. Show how to connect the following ROM chip to the 68HC11. The chip is 4 kBytes in size and will occupy memory locations $F000 to $FFFF in the memory map of the 68HC11. 4 pts each

   a. How many address bits does the chip have?

16 12 bits "11" -2

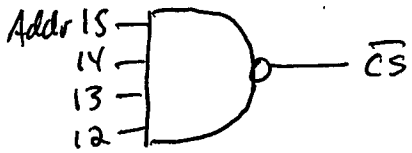
   b. Does it need access to the R/W signal? Why or why not?

No - read-only! (Also: Yes - enables output)

   c. What is the bit pattern of the most significant address bits that indicates an access to the ROM chip? (That is, what pattern of address bits is always asserted when ROM is being accessed?)

Addr = $FXXX
1st 4 bits all equal '1'

   d. Draw a diagram of a logic gate that can use the bit pattern you found in part 'c' to drive the active-low chip select for the ROM part.



16 6. Design an interrupt service routine to perform the following operation.

   a. The 68HC11 has a 2^{23} Hz crystal and the design is supposed to have one timer overflow every 4pts 500 ms (0.5s). What should the setting of the PR1 and PR0 bits be?

11

   b. Write the interrupt service routine to do the following: When a timer overflow event occurs, clear the timer overflow flag and increment memory location $C200. (Hint: What instruction 12pts should always be at the end of an interrupt service routine?)

```
LDAA  #$80
STAA  $1025
INC   $C200
RTI
```

3pts/line

used 'x' to inc $C200 -0
gibberish -9
wrote '0' to clear -3
List of 'what to do' -5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1