

(A)

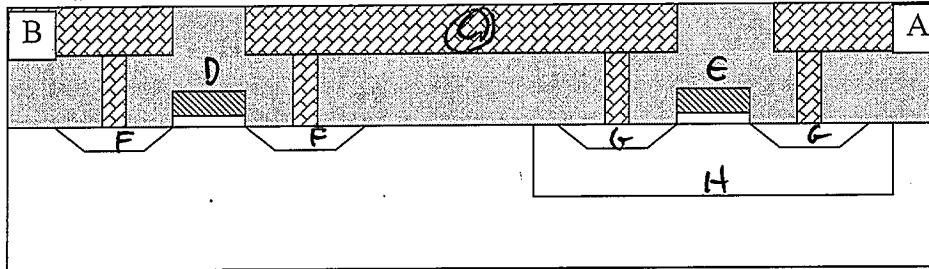
EE 534 VLSI Systems – Final Exam – Fall 2007 Name: _____

You have two hours to work this test. This exam is *open books, open notes*. However, you may not share materials or calculators during the exam!

30
pts

Problem 1: MOSFET basics, Devices, Inverter Structure

a. Label the parts of the inverter shown below.

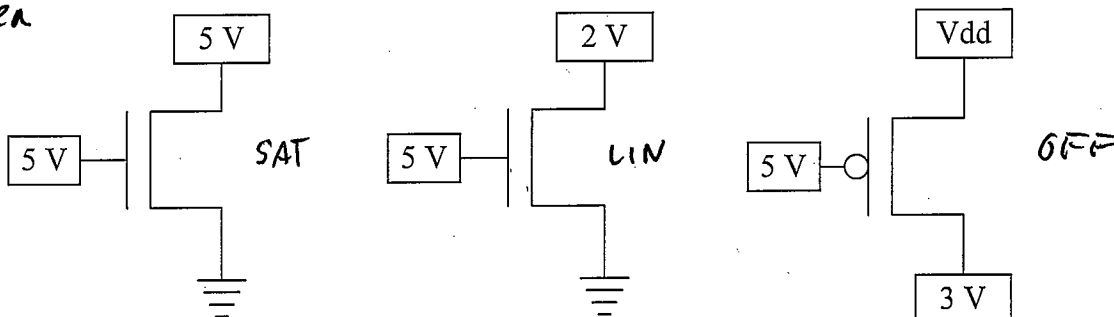


1 pt
ea

Ltr.	Part of circuit
A	GND connection <i>VDD</i>
B	VDD connection <i>GND</i>
C	Output
D	NMOS gate
E	PMOS gate
F	NMOS N diffusion
G	PMOS P diffusion
H	PMOS N-well

b. For the transistors shown below, indicate whether they are "Off", "Saturation", or "Linear." Note that both P and N transistors are shown. $V_{T,n} = 1V$, $V_{T,p} = -1V$, and V_{dd} is 5V.

2 pts
ea



c. A circuit with $V_{dd}=3.3V$ is measured in the lab to have $V_{OH} = 2.9V$ and $V_{OL} = 0.3V$ (due to loading). It is driving an input with $V_{IH} = 2.7V$ and a $V_{IL} = 0.5V$. Compute the NM_H and NM_L of the circuit.

6 pts

$NM_H = 0.2V$

$NM_L = 0.2V$

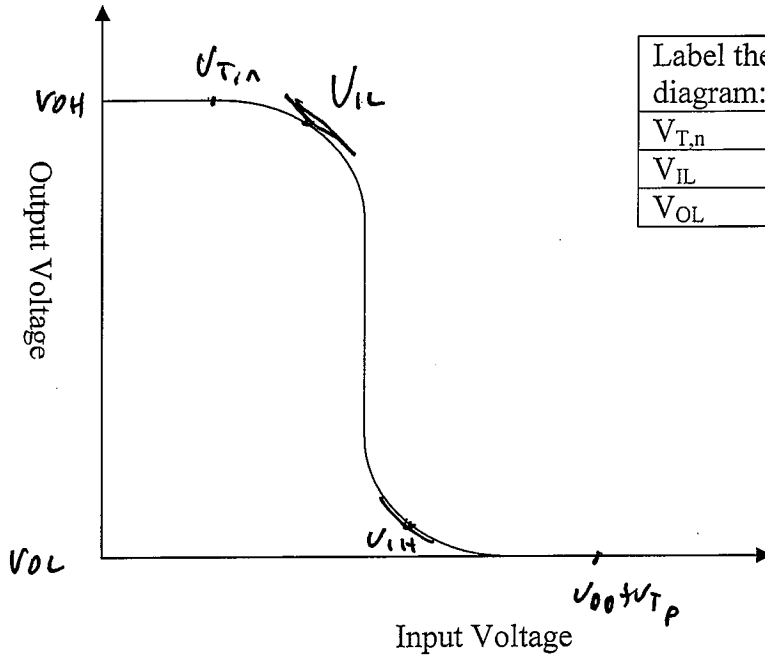
d. Will the circuit in c work correctly? Why or why not?

0pts

Yes NM's 20

e. Label the following CMOS inverter V_{in} vs. V_{out} diagram:

1ea



Problem 2: Gate performance

a. What can be done to increase a logic gate's τ_{PHL} ?

20 6 \uparrow increase, not decrease: $-C$

Raise C_{LOAD}
~~lower~~ Lower k_n
 Lower $V_{DD} - V_T$
 Raise V_T

b. Intel announced a major breakthrough in 45 nm, the introduction of a new gate-oxide material that *increases* gate-oxide capacitance. Why did they want to increase capacitance?

6 Increase cap = Increase k_n = Lower τ_p

c. Consider field oxide, the insulation layer formed away from active logic gates. Should the capacitance of field oxide be maximized or minimized, and why?

0 Minimized - that capacitance only slows down signals

Problem 3: Power Dissipation and Fab Technology

Jumble - 10
got close
+ 10 out
- 5

20

- a. The ASIC department designed a 90 nm ASIC. It had a core voltage of 1.0V, a clock frequency of 800 MHz, and each gate drove an average load of 10 fF (femtofarads). The ASIC had a measured power dissipation of ~~20~~ Watts. The ASIC department now wants to do a "die shrink" on the ASIC and move the same ASIC into a 65 nm process. The new process will have a core voltage of 1.2V, a clock frequency of 1 GHz, and each gate will drive an average load of 8 fF. Given the old power dissipation of 20 Watts (and the same number of gates and the same duty cycle), estimate the power dissipation of the ASIC after the "die shrink" (that is, after moving from 90 nm to 65 nm).

off by 10 - 2

$$\frac{P_{diss2}}{P_{diss1}} = \frac{1000 \cdot 8 \cdot 1.2^2}{800 \cdot 10 \cdot 1.0^2} \cdot 20 = 1.44 \cdot 20 = 28.8 \text{ W}$$

wrong test: -20

- b. Intel Corporation launched its new 45 nm fab line this month. According to Moore's law, when should they plan to launch their 22 nm fab line?

18 mos. later

Problem 4: Testability and Chip Packaging

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- a. Identify whether the following cases are a *fault* or a *failure*, and explain your answer.

1 - A car's spare tire is flat. *fault - problem that isn't observed*

2 - The tire on the front right of the car is flat. *failure*

- b. What is the minimum number of test vectors needed to test a 4-input, 3-output logic circuit?

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- c. Compare flip-chip bonding to wire bonding: Which one has the lowest resistance and inductance?

flip-chip

- d. Define *multi-chip module*. *multiple IC's in a single package*

2

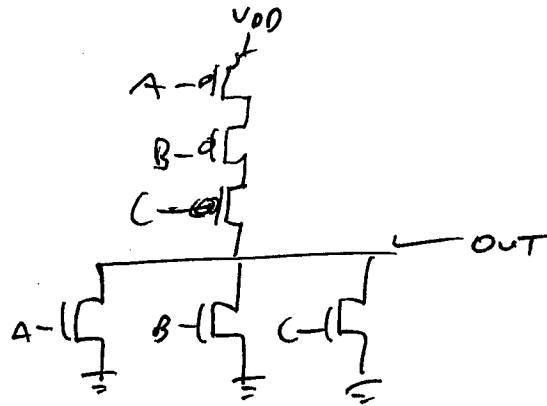
Problem 4: Complex Gate Design

- 20 a. Consider a 3-input NOR gate. How many N and P transistors does it have if it is implemented in static CMOS, dynamic CMOS, and domino logic?

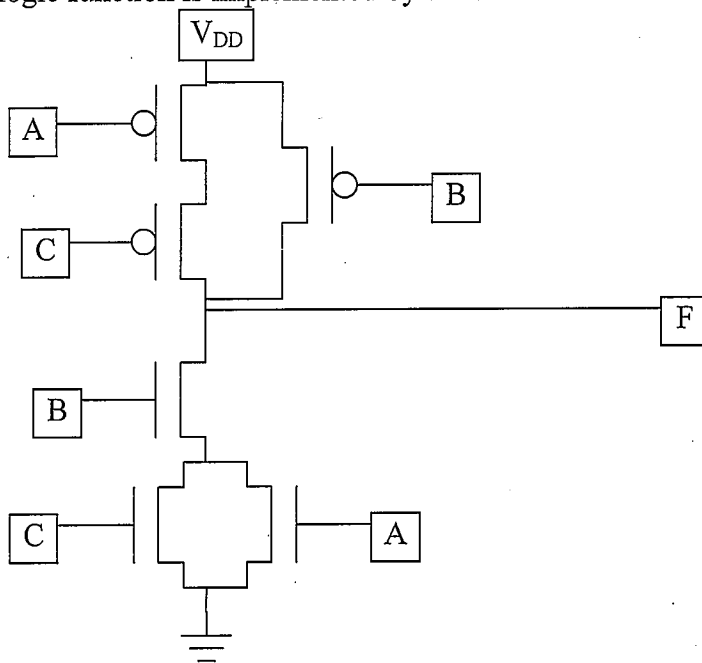
6	5	7
3N	4N	5N
3P	1P	2P

each

- b. Draw a schematic for the gate in part a using static CMOS logic.



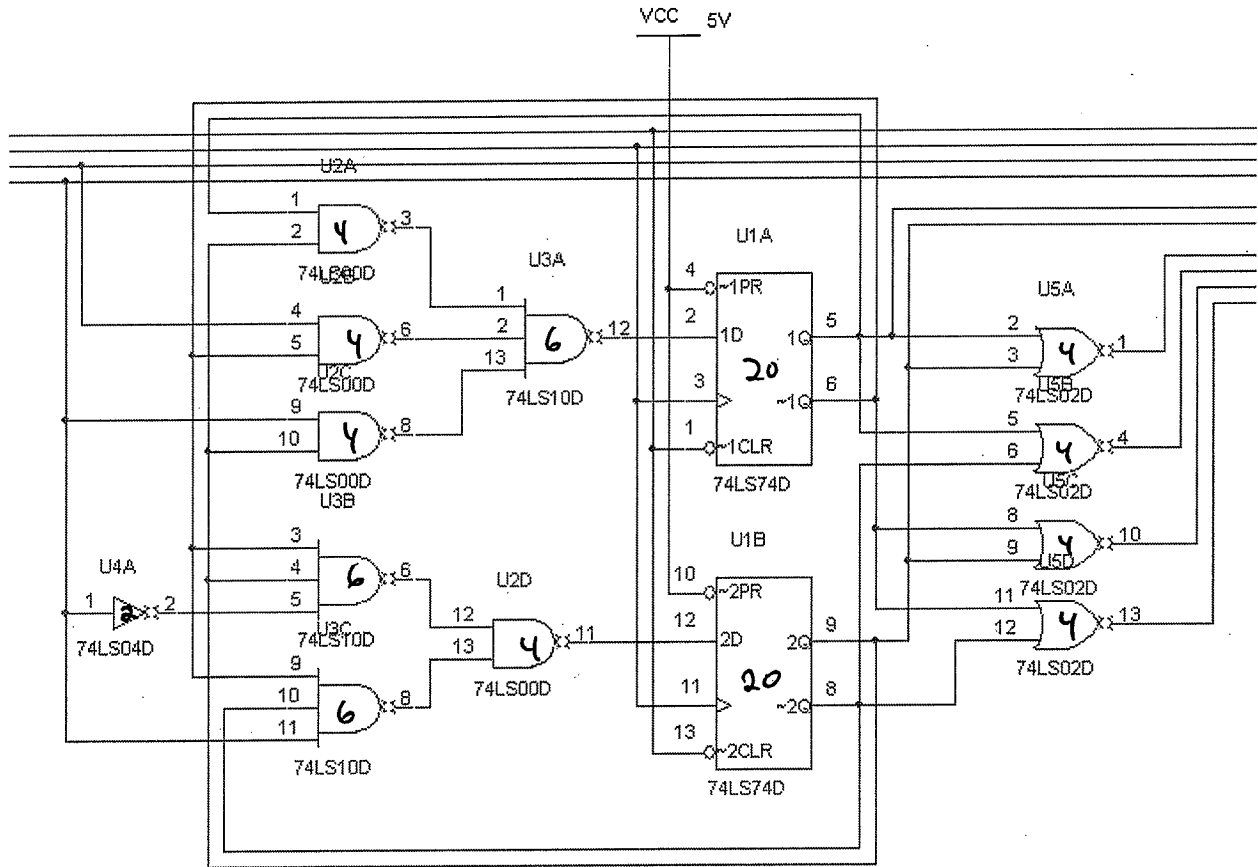
- c. What logic function is implemented by the schematic below?



$$F = \neg (B \cdot (A + C))$$

16 pts
5

- d. Estimate the transistor count of the following circuit. Assume a static CMOS implementation and that the DFF circuit has 20 transistors. Note that all gates have inverted outputs. That is, the circuit is made of inverters, NAND gates, NOR gates, and 2 DFFs.



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