

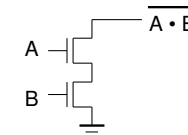
EE534
VLSI Design System

Lecture 9:Chapter 7

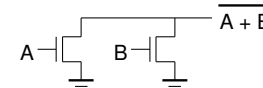
CMOS Equivalent inverter and layout

Review: Construction of PDN

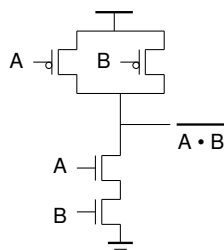
□ NMOS devices in **series** implement a NAND function



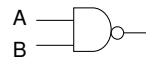
□ NMOS devices in **parallel** implement a NOR function



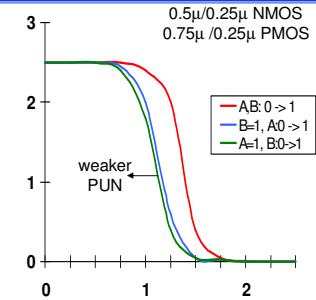
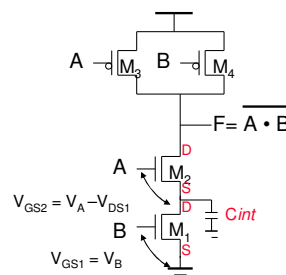
Review: CMOS NAND



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



Review: VTC is Data-Dependent



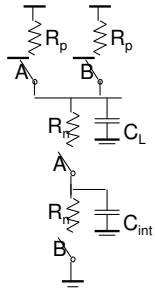
□ The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$$V_{Tn1} = V_{Tn0}$$

$$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{|2\phi_F| + V_{int}} - \sqrt{|2\phi_F|})$$

since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C_{int}

Input Pattern Effects on Delay-I

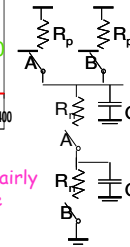
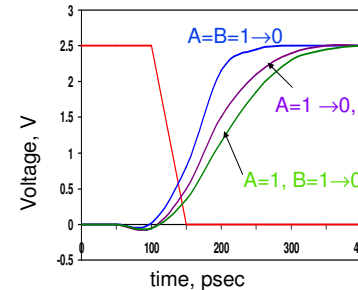


- Delay is dependent on the **pattern** of inputs
- Low to high transition
 - both inputs go low
 - delay is $0.69 R_p/2 C_L$ since two p-resistors are on in parallel
 - one input goes low
 - delay is $0.69 R_p C_L$
- High to low transition
 - both inputs go high
 - delay is $0.69 2R_n C_L$
- Adding transistors in series (without sizing) slows down the circuit

Delay Dependence on Input Patterns-II

The reason for difference in low to high transition is due to internal node capacitance and high to low is due to initial state of the internal nodes.

2-input NAND with
 NMOS = $0.5\mu\text{m}/0.25\mu\text{m}$
 PMOS = $0.75\mu\text{m}/0.25\mu\text{m}$
 $C_L = 10\text{ fF}$



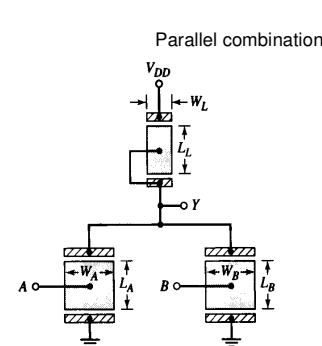
Input Data Pattern	Delay (psec)
A=B=0→1	69
A=1, B=0→1	62
A=0→1, B=1	50
A=B=1→0	35
A=1, B=1→0	76
A=1→0, B=1	57

Conclusions: Estimates of delay can be fairly complex - have to consider internal node capacitances and the data patterns

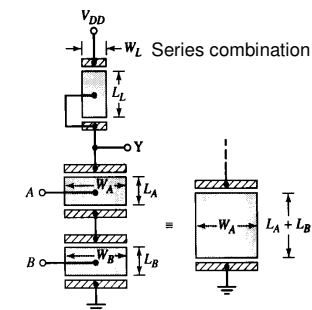
CMOS gate design

- Designing a CMOS gate:
 - Find **pulldown** NMOS network from logic function or by inspection
 - Find **pullup** PMOS network
 - By inspection
 - Using logic function
 - Using dual network approach
 - Size transistors using equivalent inverter
 - Find **worst-case** pullup and pulldown paths
 - Size to meet rise/fall or threshold requirements

Equivalent inverter: effective width to length ratios (model I)



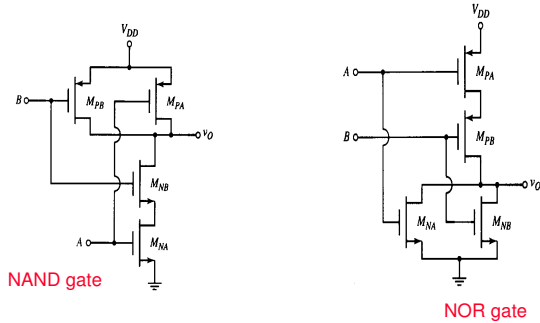
For the **NOR gate** the **effective width of the driver transistors doubles**. That means the effective aspect ratio is increased.



For the **NAND gate** the **effective length of the driver transistors doubles**. That means the effective aspect ratio is decreased.

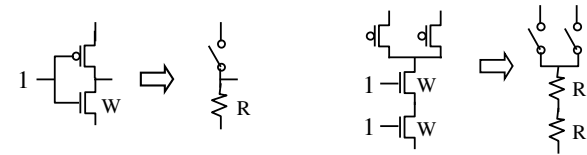
Exercise: Design and compare two input NAND and NOR gates

- Find W/L relationship between NMOS and PMOS transistors
- Assume $K'n=2K'_p$



Analysis of CMOS gates

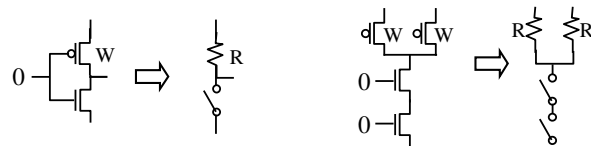
- Represent “on” transistors as resistors



- Transistors in series → resistances in series
 - Effective resistance = $2R$
 - Effective width = $\frac{1}{2} W$

Analysis of CMOS gates, cont

- Represent “on” transistors as resistors



- Transistors in parallel → resistances in parallel
 - Effective resistance = $\frac{1}{2} R$
 - Effective width = $2W$

Equivalent Inverter

- CMOS gates: many paths to Vcc and Gnd
 - Multiple values for V_{TH} , V_{IL} , V_{OL} , etc
 - Different delays for each input combination
- Equivalent inverter
 - Represent each gate as an inverter with appropriate device width
 - Include only transistors which are on or switching
 - Calculate V_{TH} , delays, etc using inverter equations

Static CMOS Logic Characteristics

- For V_{TH} , the V_{TH} of the equivalent inverter is used (assumes all inputs are tied together)
 - For specific input patterns, V_{TH} will be different
- For V_{IL} and V_{IH} , only the **worst case is interesting since circuits must be designed for worst-case noise margin**
- For delays, both the maximum and minimum must be accounted for in race analysis

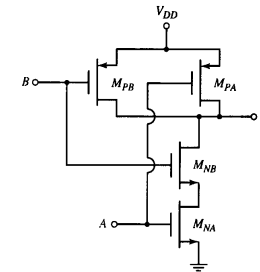
Equivalent Inverter: V_{TH}

- Example: NAND gate threshold V_{TH}

Three possibilities:

- A & B switch together
- A switches alone
- B switches alone

- What is equivalent inverter for each case?



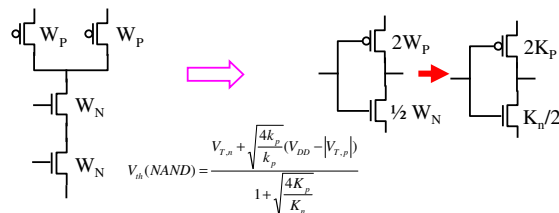
A	B	v_O
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

CMOS NAND gate and its inverter equivalent

- Can we estimate switching threshold of the NAND gate by using CMOS inverter expression for the switching threshold?

$$V_{th}(INR) = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{K_p}{K_n}}}$$

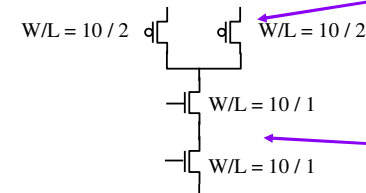
If $K_n=K_p$, $V_{th}=?$



NAND Example

- A 2-input NAND gate is driving 0.01 pF load. Estimate t_{pLH} and t_{pHL} assuming both inputs switching at the same time. Use the following device parameters:

- $K'_n = 20 \mu A/V^2$
- $K'_p = 10 \mu A/V^2$
- $V_{Tn} = |V_{Tp}| = 1.0V$
- PMOS: $W=10 \mu m$, $L_{eff}=2 \mu m$
- NMOS: $W=10 \mu m$, $L_{eff}=1 \mu m$



Driving High:
PMOS in Parallel:
Effective $W/L = (10 + 10) / 2 = 10/1$

Driving Low:
NMOS in Series:
Effective $W/L = 10 / (1+1) = 5/1$

Solution to Example

SOLUTION:

The delay can be calculated using an equivalent inverter of the NAND gate. From equations (6.22b) and (6.23b), we obtain:

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

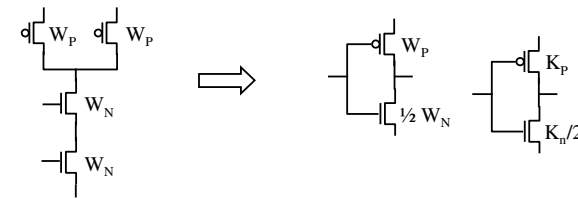
$$= \frac{0.01 \times 10^{-12}}{20 \times 10^{-6} \cdot 5/1 \cdot (5-1)} \left[\frac{2}{4} + \ln \left(\frac{4 \times 4}{5} - 1 \right) \right] = 32.2 \text{ ps}$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - V_{T,p})} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

$$= \frac{0.01 \times 10^{-12}}{10 \mu\text{A} \cdot 10/1 \cdot (5-1)} \left[\frac{2}{4} + \ln \left(\frac{4 \times 4}{5} - 1 \right) \right] = 32.2 \text{ ps}$$

Equivalent inverter: Worse case delay design consideration

- Represent complex gate as inverter for delay estimation
- Use worst-case delays
- Example: NAND gate
 - Worst-case (slowest) pull-up: only 1 PMOS "on"
 - Pull-down: both NMOS "on"



CMOS NOR gate: design consideration

$$V_{th}(INR) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}(V_{DD} - |V_{T,p}|)}}{1 + \sqrt{\frac{K_p}{4K_n}}}$$

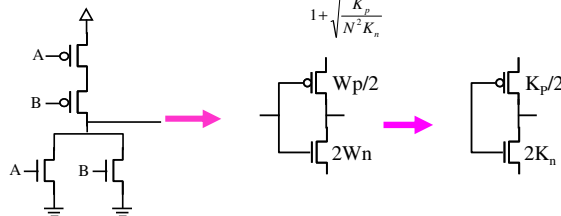
Two input

$$V_{th}(INR) = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n}(V_{DD} - |V_{T,p}|)}}{1 + \sqrt{\frac{K_p}{K_n}}}$$

One input

$$V_{th}(INR) = \frac{V_{T,n} + \sqrt{\frac{k_p}{N^2 k_n}(V_{DD} - |V_{T,p}|)}}{1 + \sqrt{\frac{K_p}{N^2 K_n}}}$$

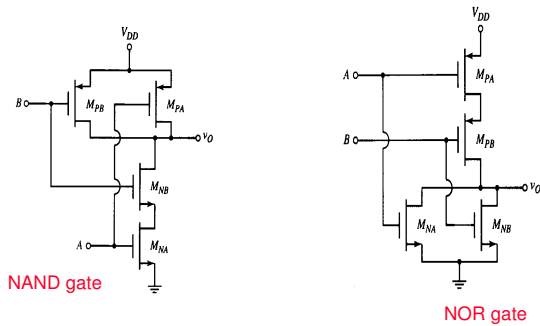
For N inputs



Equivalent inverter

- Problems with equivalent inverter method:
 - Need to take into account load capacitance C_L
 - Depends on number of transistors connected to output (junction capacitances)
 - Even transistors which are off (not included in equivalent inverter) contribute to capacitance
 - Need to include capacitance in intermediate stack nodes. Worse-case: need to charge/discharge all nodes
 - Body effect of stacked transistors

Transistor Sizing



Transistor sizing: an approach

- If MOSFET serially connected in a current path, the overall current path resistance will be

$$R = \frac{R_s L_1}{W_1} + \frac{R_s L_2}{W_2} + \frac{R_s L_3}{W_3} + \dots$$

$$R = R_s \left(\frac{L_1}{W_1} + \frac{L_2}{W_2} + \frac{L_3}{W_3} + \dots \right)$$

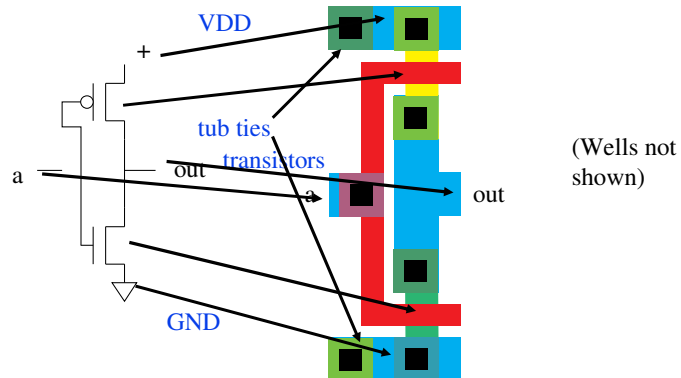
- All serially connected MOSFET can be replace with a single MOSFET as

$$\frac{L_{eq}}{W_{eq}} = \frac{W_1}{L_1} + \frac{W_2}{L_2} + \frac{W_3}{L_3} + \dots$$

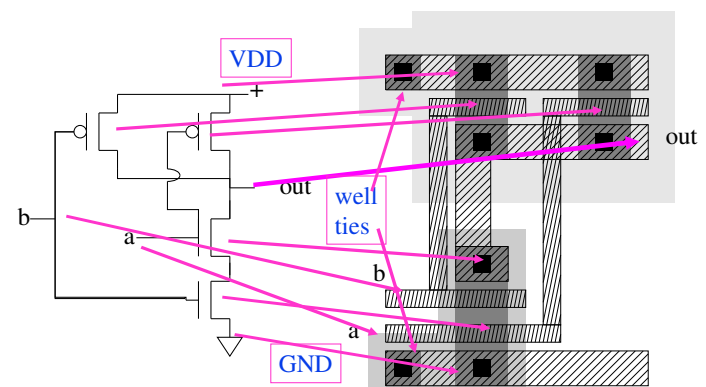
If the MOSFET are connected in parallel combination then,

$$\frac{L_{eq}}{W_{eq}} = \frac{1}{\frac{W_1}{L_1} + \frac{W_2}{L_2} + \frac{W_3}{L_3} + \dots}$$

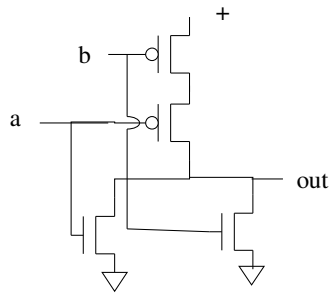
Review: Inverter layout



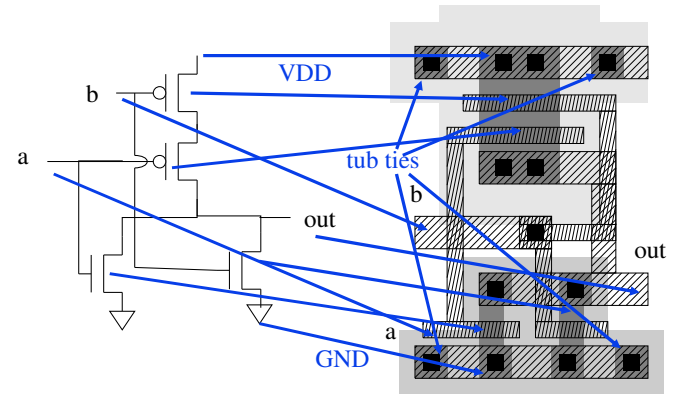
NAND layout



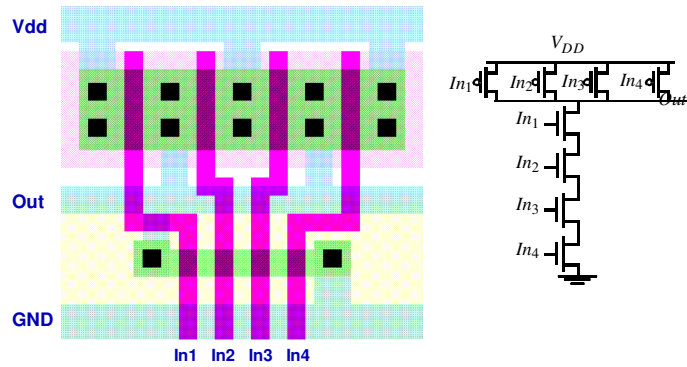
NOR gate



NOR layout

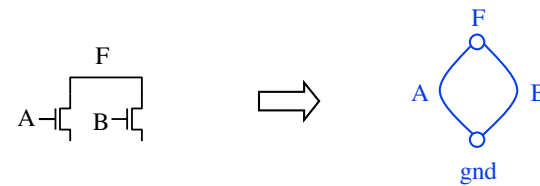


4-input NAND Gate



Graph-based dual network

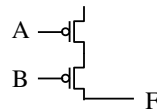
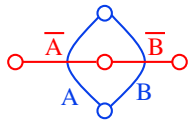
- Draw network for PUN or PDN
 - Circuit nodes are vertices
 - Transistors are edges



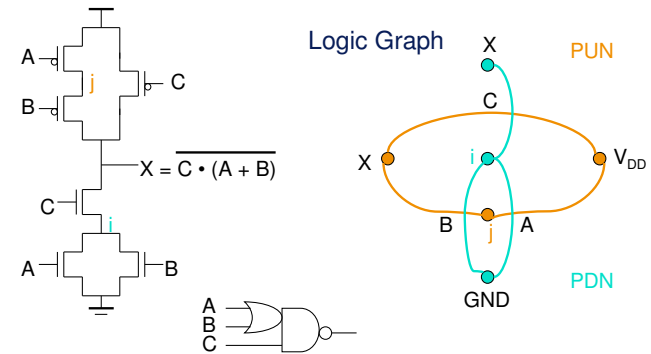
Graph-based dual network (2)

To derive dual network:

- Create new node in each enclosed region of graph
- Draw new edge intersecting each original edge
- Edge is controlled by inverted input

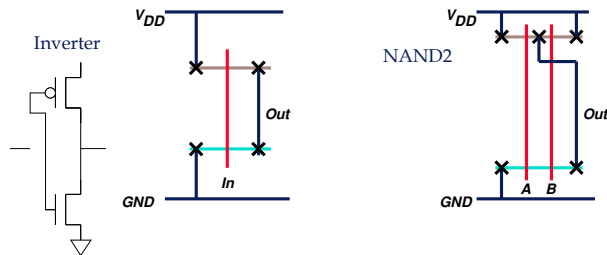


Dual Graph concept



Stick Diagrams

Contains no dimensions
Represents relative positions of transistors



CMOS gate layout

- Goal: minimum area
- Method
 - Minimize diffusion breaks (reduces capacitance on internal nodes)
 - Align transistors with common gates above each other in layout (minimizes poly length)
 - Group PMOS and NMOS transistors together
- Approach:
 - Use Euler path method to find ordering of transistors in layout

Layout: Euler path method

- **Goal:** layout without diffusion breaks
- Method for finding ordering of transistors in layout → **Euler path**
 - Euler path → path through a graph that traverses each edge only once
 - Find **common Euler path** in pullup and pulldown graph
 - This gives the ordering of inputs in the layout

Complex CMOS logic gates

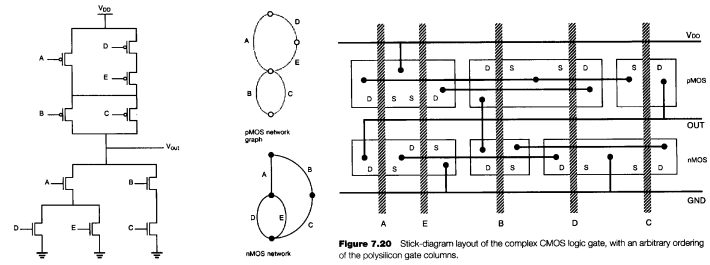
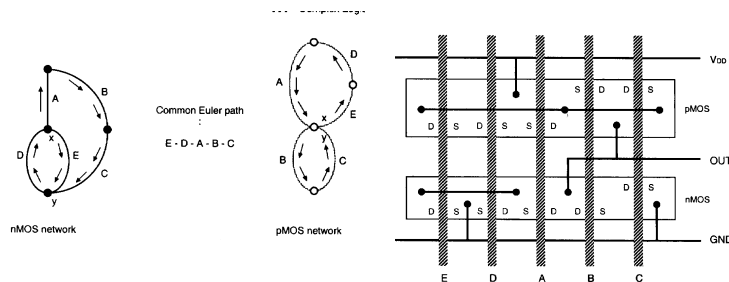


Figure 7.20 Stick-diagram layout of the complex CMOS logic gate, with an arbitrary ordering of the polysilicon gate columns.

Complex CMOS logic gates



Another Layout Example

- Start with...

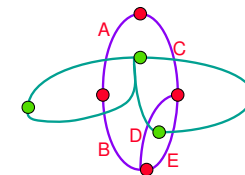
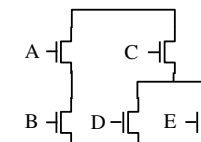
PDN (by inspection):

$$F = (\overline{C} + \overline{DE}) \cdot (\overline{A} + \overline{B})$$

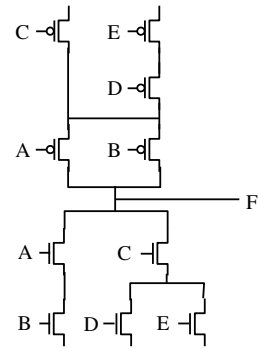
$$F = (\overline{C} + [D + E]) \cdot (\overline{AB})$$

$$F = (\overline{C} \cdot [D + E]) \cdot (\overline{AB})$$

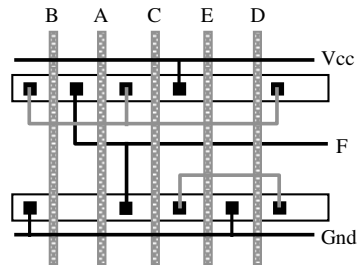
$$F = (\overline{AB} + C \cdot [D + E])$$



Layout: Euler path method

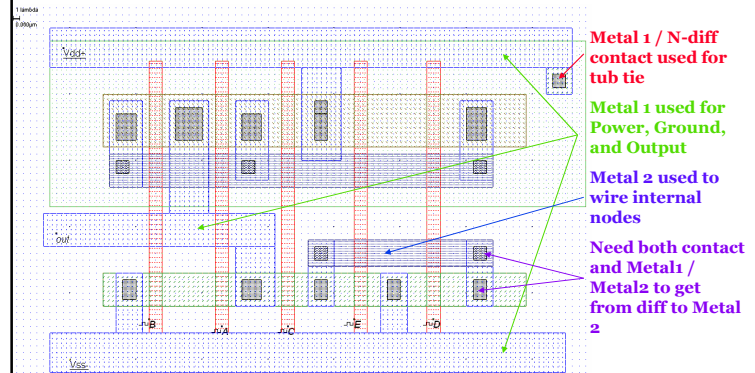


Euler path: B→A→C→E→D



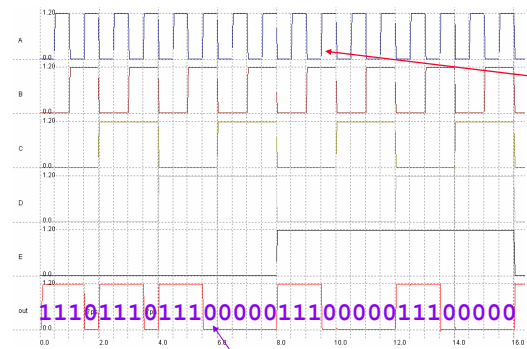
1. Order transistors gates according to Euler path
2. Connect Vcc and Gnd
3. Make other connections according to circuit diagram

Layout continued...



If you flip back and forth, you will see how the layout implements the stick diagram. Note the input order and the topology both match.

But does it work?



Set inputs on power-of-2 boundaries to generate entire counting pattern

You can read the truth table directly off of the output row!