

# EE534 Project Guidelines

In addition to producing a working logic gate, the work performed in projects should produce logic gates with a “professional” appearance. In order to clarify the process, the following rubric is going to be used to evaluate the project reports.

## Rubric 1: Projects 1 and 2

Projects 1 and 2 require the design of single logic gates. The goal of project 1 is to design a static CMOS logic gate and the goal of project 2 is to design the same gate in dynamic CMOS. You need to hand in a cover page that lists the gate and the project members, a 1-page image of the layout, and a 1-page image of the simulation. The simulation and layout will be graded as follows.

### Gate Layout:

Gate layout appears correct (arrangement and interconnection of N and P-channel devices).....	20 points
No design rule errors (must see message at bottom of print-out) .....	10 points
Layout is printed on white background.....	5 points
Vdd and Vss are each routed on a single, continuous, horizontal piece of Metal 1.....	5 points
There is only one N well .....	5 points
N and P diffusions are aligned horizontally.....	5 points
Inputs are routed in Polysilicon and stretch all the way from top to bottom .....	5 points
Output is routed on Metal 1 .....	5 points
There is a single contact to polarize the N well from Vss (Metal 1).....	5 points

### Simulation:

All possible input combinations are applied to the gate .....	10 points
Gate works correctly .....	20 points
Simulation is printed on white background .....	5 points

Total..... 100 points

## Rubric 2: Project 3 – See next page

## Rubric 2: Project 3

Project 3 requires the design of a more complicated logic structure. You need to hand in a complete report on the design and deliver an oral presentation in class using PowerPoint or equivalent software. The report needs to cover the desired function of the circuit, explain the design (usually in the form of a circuit schematic and accompanying text), and present layout and simulation results. A “circuit schematic” is a transistor-level diagram of the complete circuit. The schematic can be hand-drawn, although computer-drawn is preferred. The oral presentation needs to cover the same material and should last about 5 minutes.

Project 3 will be graded as follows.

### Gate Layout:

Gate layout appears correct (arrangement and interconnection of N and P-channel devices)..... 10 points  
No design rule errors (must see message at bottom of print-out) ..... 10 points  
Layout is printed on white background..... 5 points

### Simulation:

Enough input combinations are applied to the circuit to demonstrate correct function..... 10 points  
Circuit works correctly ..... 10 points  
Simulation is printed on white background ..... 5 points

### Written Report

Report handed in on time ..... 10 points  
Report includes description of circuit function, description of design (circuit schematic), and simulation results ..... 10 points  
Circuit schematic appears correct (arrangement and interconnection of transistors) ..... 10 points

### Oral Presentation

Presentation is clear and lasts 4-5 minutes..... 10 points  
Presentation covers function, design, layout, and simulation ..... 10 points

Total ..... 100 points